FIG.1

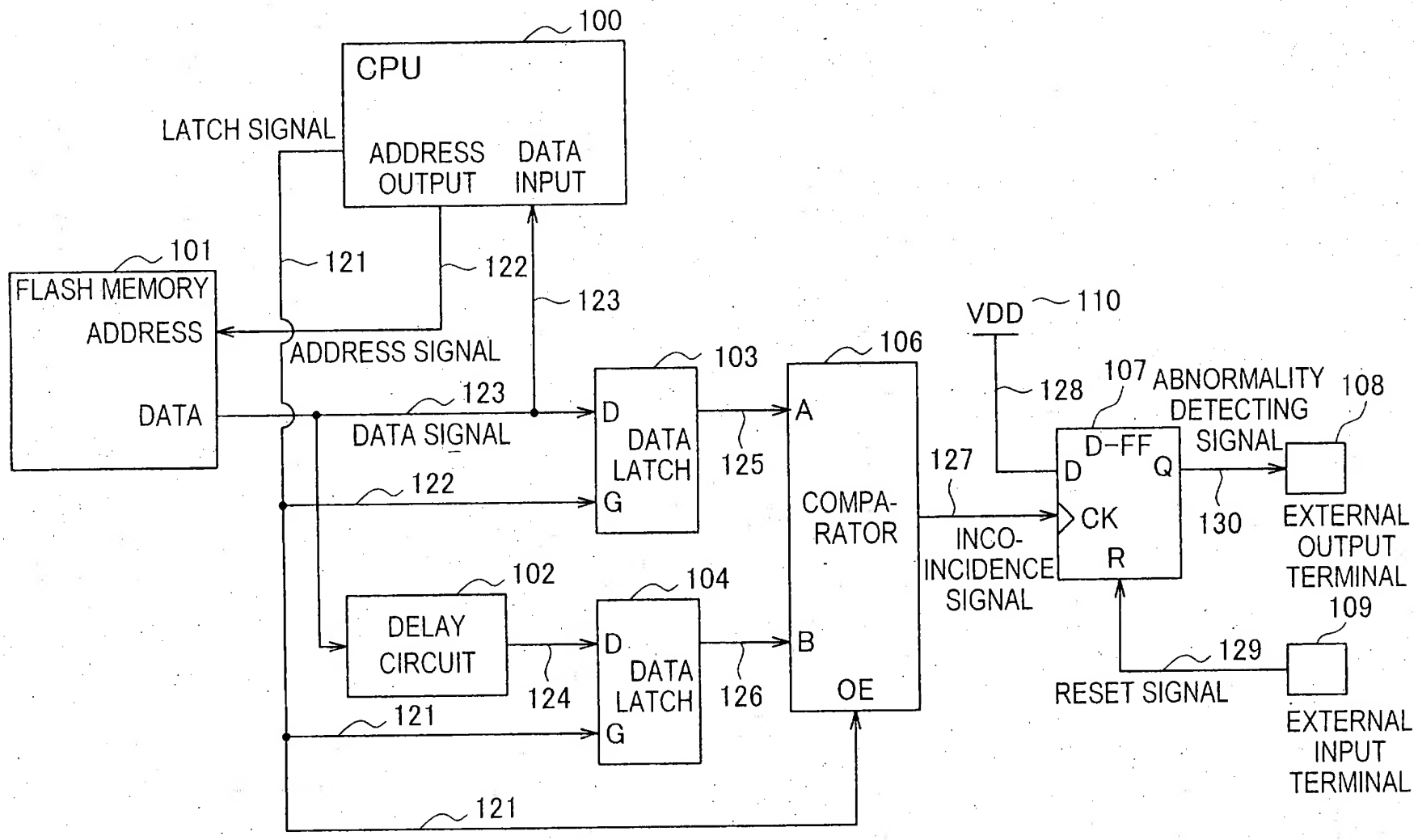

100
CPU
LATCH SIGNAL
ADDRESS OUTPUT
DATA INPUT
101
FLASH MEMORY
ADDRESS
DATA
121
122
123
ADDRESS SIGNAL
123
DATA SIGNAL
103
D
DATA LATCH
G
125
106
A
COMPA-RATOR
B
OE
VDD
110
128
107
D-FF
D
Q
CK
R
127
INCO-INCIDENCE SIGNAL
ABNORMALITY DETECTING SIGNAL
108
130
EXTERNAL OUTPUT TERMINAL
109
129
RESET SIGNAL
EXTERNAL INPUT TERMINAL
122
102
DELAY CIRCUIT
124
104
D
DATA LATCH
G
126
121
121

FIG.2

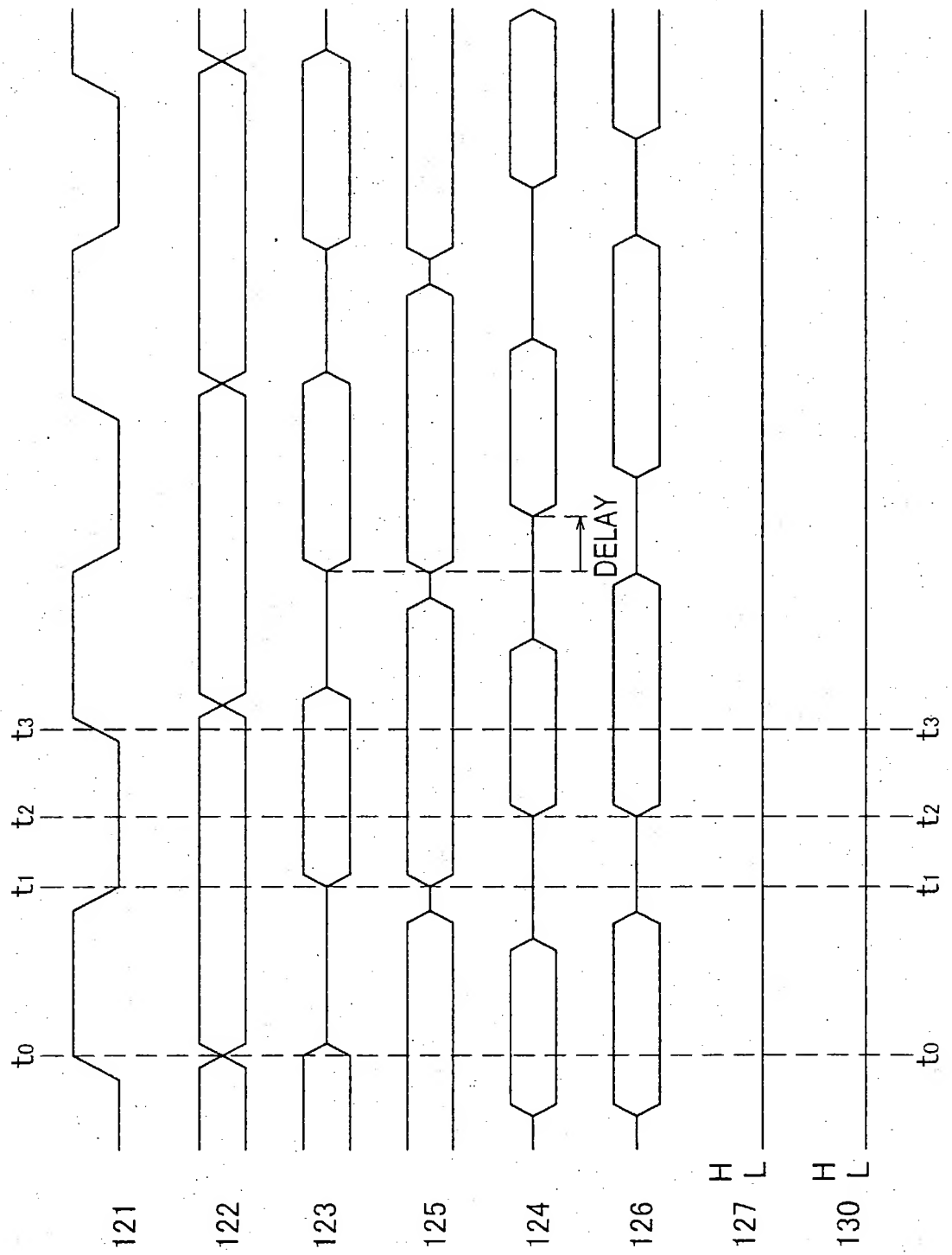


FIG.3

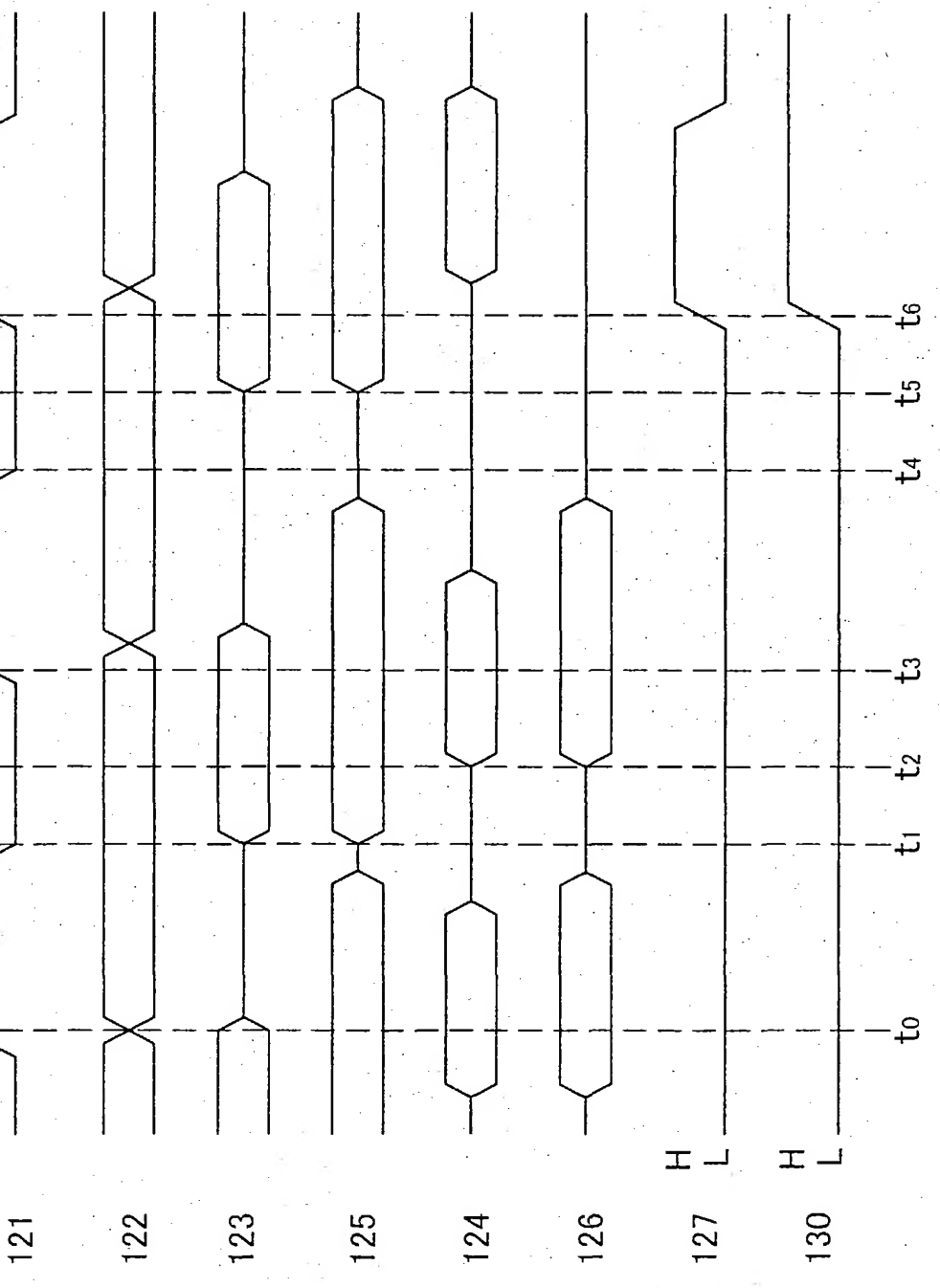


FIG.4

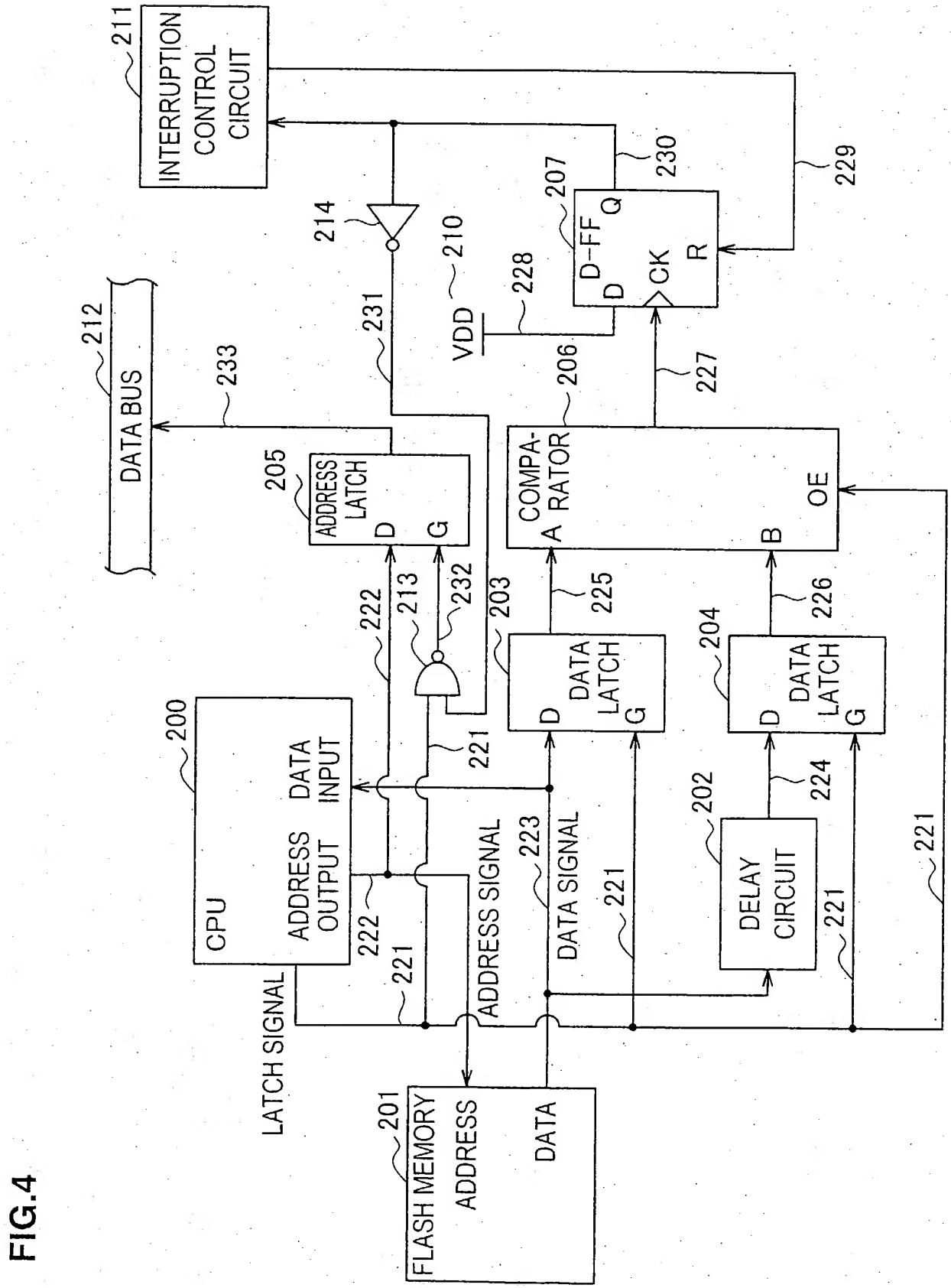
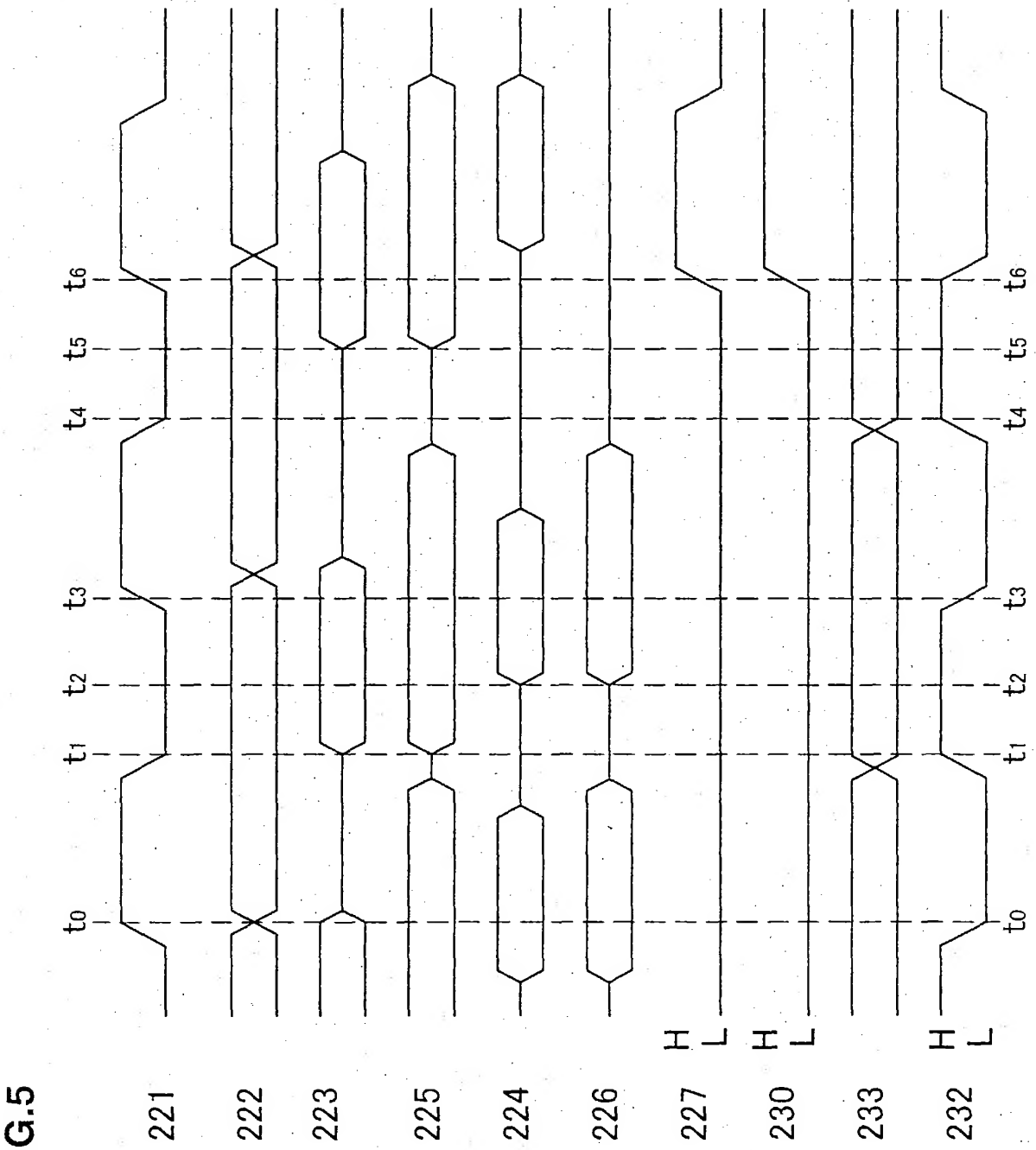

211
INTERRUPTION CONTROL CIRCUIT
214
210
207
D-FF
D
CK
Q
R
230
229
231
VDD
228
212
DATA BUS
233
206
227
205
ADDRESS LATCH
D
G
COMPA-RATOR
A
B
OE
222
213
232
203
225
226
204
200
CPU
ADDRESS OUTPUT
DATA INPUT
221
DATA LATCH
D
G
DELAY CIRCUIT
202
224
LATCH SIGNAL
ADDRESS SIGNAL
DATA SIGNAL
223
201
FLASH MEMORY
ADDRESS
DATA

FIG.5


221
222
223
225
224
226
227
230
233
232
H
L
H
L
H
L
t0
t1
t2
t3
t4
t5
t6
t0
t1
t2
t3
t4
t5
t6